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A Low Power Front-end Architecture for SiPM Readout with Integrated ADC and Multiplexed Readout

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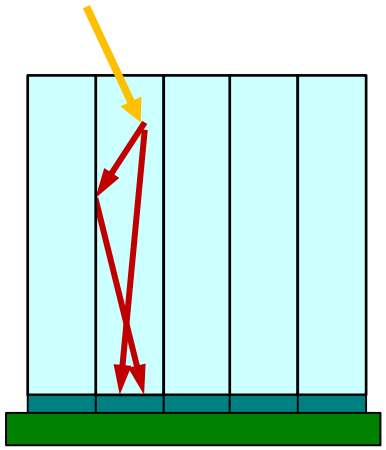
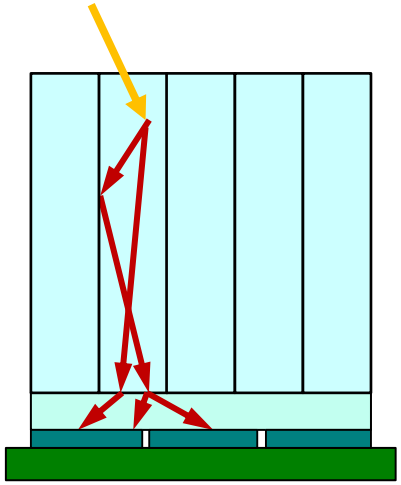
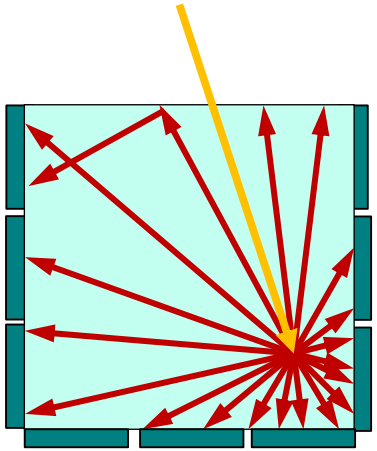
Schaltungstechnik
und Simulation

Talk Outline

- Detector readout with SiPMs
- Front-end requirements
- Single-ended front-end designs
- Chip architecture
- Measurement results

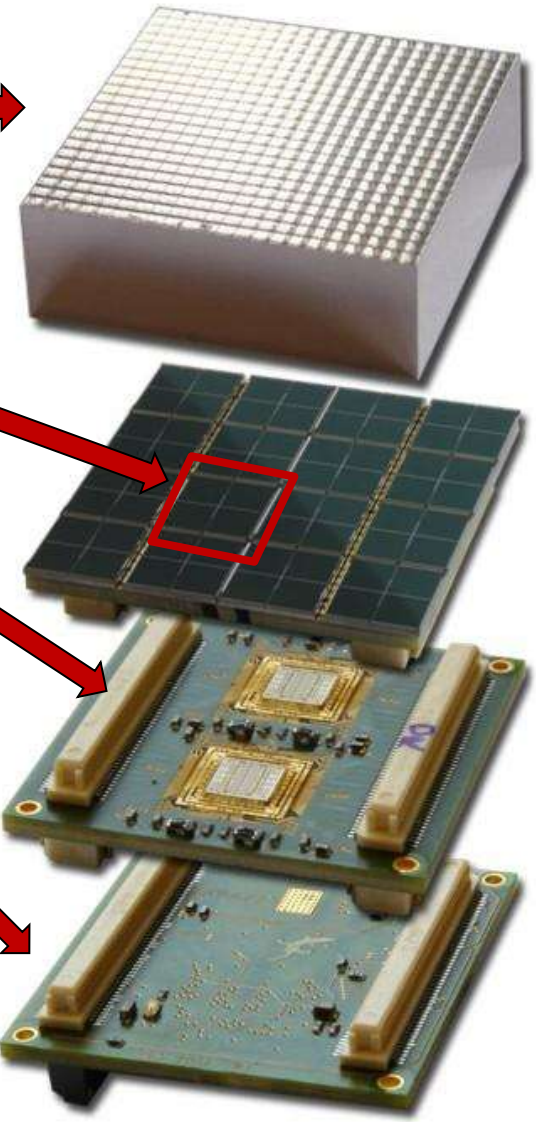
Crystal Readout with SiPM

- Scintillator Crystals + SiPMs → excellent gamma detectors
  Application in medical imaging and particle physics experiments
- Three main concepts:

Pixelated crystals 1:1 coupling	Pixelated crystals + light sharing → Interpolation	Monolithic crystal → Interpolation
		
+ Good timing performance + Large signals + Low data rate	+ High spatial resolution – Must detect small signals – Increased data rate	+ Depth of Interaction – Must detect small signals – Largest data rate

SiPM Detector Readout: HYPERIMAGE and SUBLIMA

- HYPERIMAGE module for preclinical PET
  - Crystal block → e.g. 22×24 LYSO crystals of 1.3mm pitch
  - SiPM tile → 4×4 Monolithic SiPM arrays with 2×2 SiPMs (4×4mm2)
  - ASIC tile → 2 PETA ASICs with 36 TDC/ADC channels each
  - Interface tile → FPGA for preprocessing data



HyperImage Stack

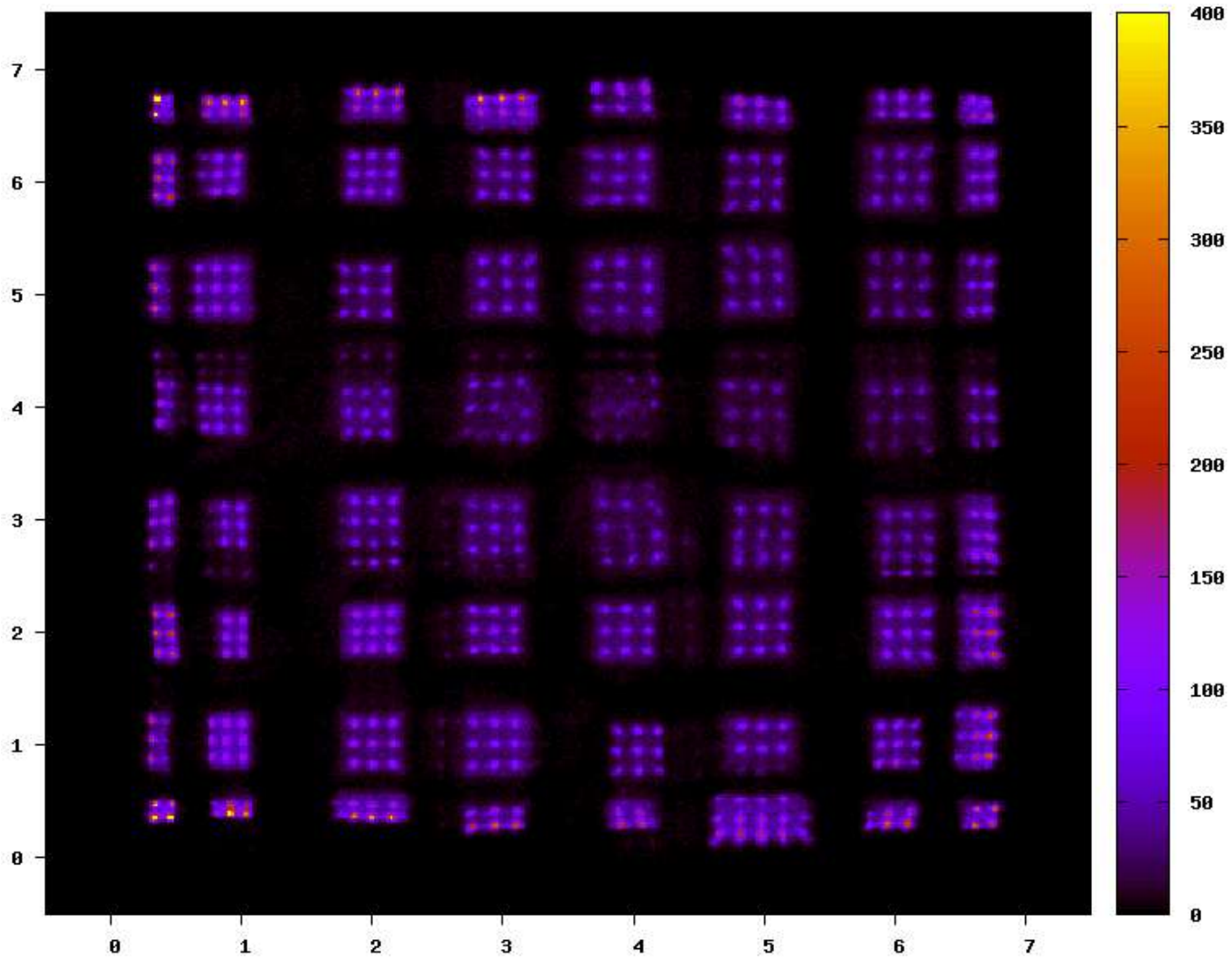
- One of the SUBLIMA goals:
  - High resolution module with 1:1 coupling
  - Excellent time resolution (c.r.t. <300ps) for ToF

- Both projects are EU funded

#241711 SUBLIMA

#201651 HYPERIMAGE

HYPERIMAGE Flood Map Result



- ^{22}Na source
- 8x8 SiPMs
  22x24 crystals
  1.3 mm x 1.3 mm
  ⇨ 3x3 per SiPM
- 15 MEvents
- 2D-Gaussian fit

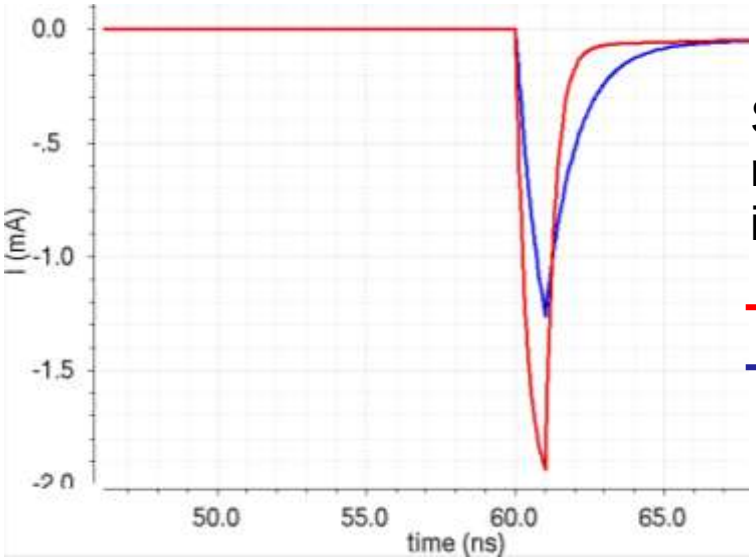
Taken in „Neighbor Trigger“ mode: The channel receiving the main fraction of the signal triggers its neighbors.

FrontEnd Requirements

- Spatial Resolution = high channel density (1:1 coupling)
  - Single-ended channels — simplified wiring
  - Low power consumption — simplified cooling
  - Single-wire output — simplified backend
- Timing Resolution
  - Low input impedance — improved SiPM response
  - Precise threshold settings — low thresholds for ‘first photon’
  - Programmable input dc potential — precise control of SiPM overvoltage
- Frequency bandwidth requirements
  - Programmable low-pass frequency — reduced noise
  - Programmable high-pass frequency — elimination of baseline fluctuations
- Low noise

Time Resolution: **Why** Low Input Impedance and **How** to get it?

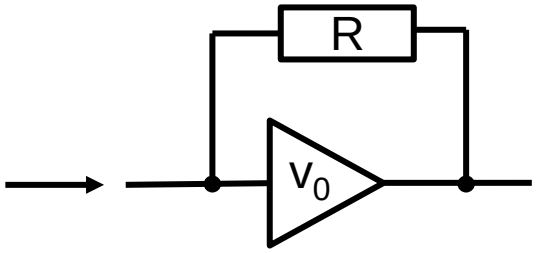
- Rise time is faster for low input impedance:

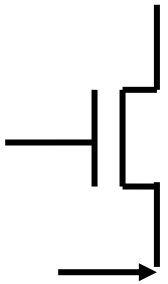


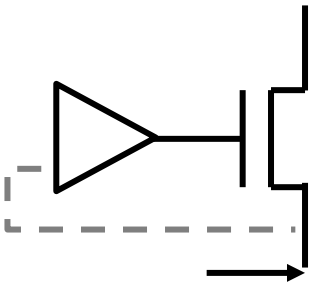
Simulation of SiPM response for two input impedances:

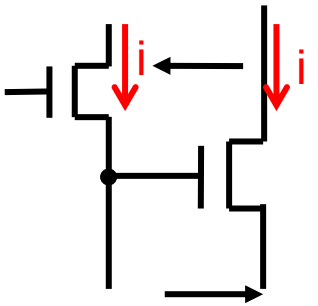
10 Ω
30 Ω

- Circuits:









TransImpedance Amplifier (TIA)
-Fixed input DC
- **Rin → R/v_0 @BW**

Grounded gate stage

Rin limited to 1/g_m

Regulated Cascode

Rin < 1/g_m
Higher power cons.

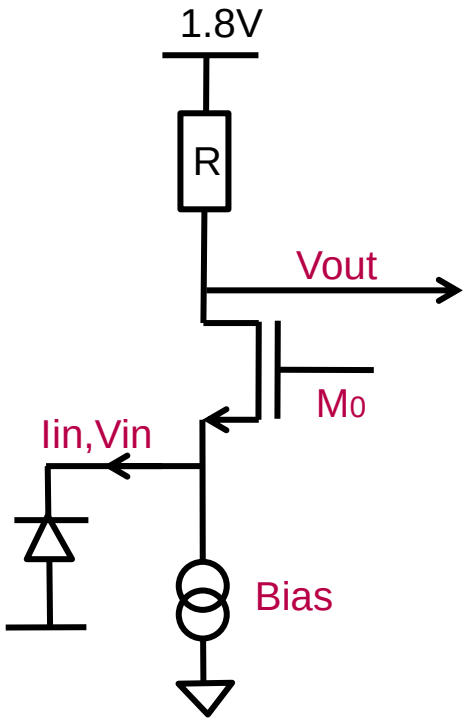
Mirror Regulation

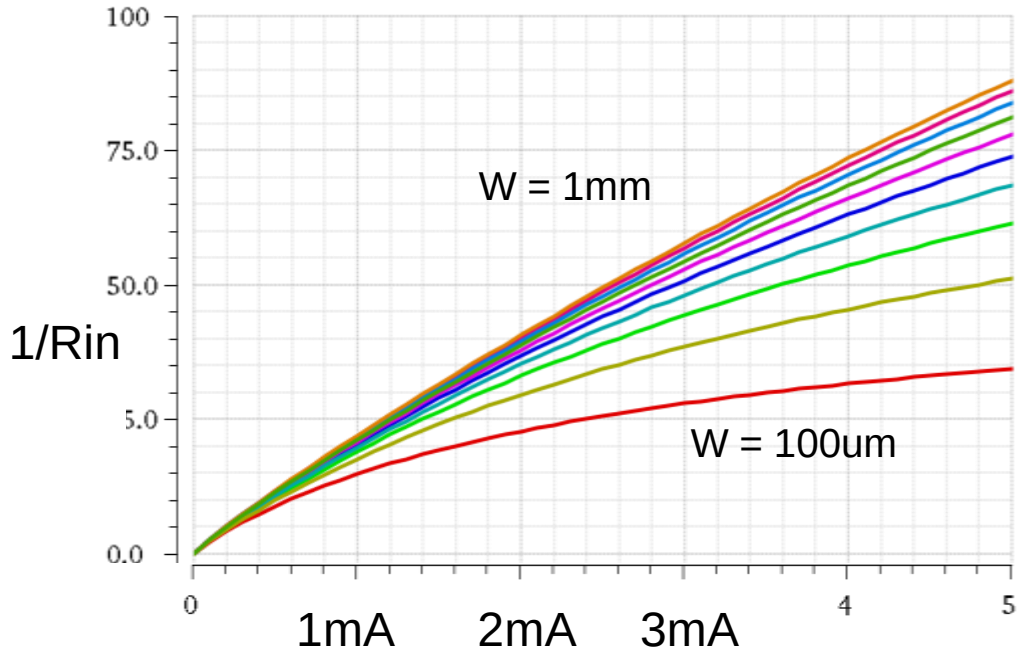
W.Shen, Uni HD
Possible instability

Input Stage Design: Simple Idea

- M_0: cascode Nmos with high g_m
- R: load resistor, I→ U gain
- Bias: current sink (~2mA)

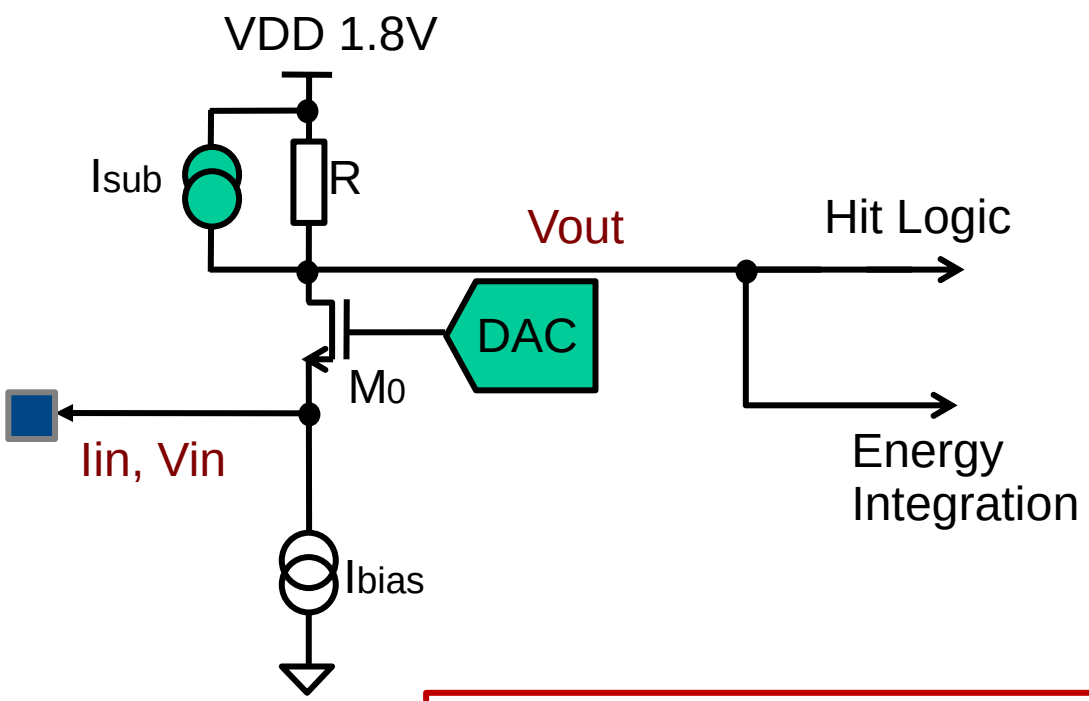
Bias = 1mA → Rin ~ 50Ω
Bias = 2mA → Rin ~ 25Ω





- Fundamental limit for MOS (weak inv. @ given current)
  (For bipolar trans.: **Rin ~ V_{Th} / I_C** ~ 25 mV / 1mA ~ 25 Ω)

Input Stage Design: (1) Straight Cascode



Sub source : compensation current
→ higher dynamic range
→ fixed Vout

DAC : 5 bit- 50mV steps per-channel
→ variable DC input (span ~ 1V)
→ variable Rin

Energy Integration: *U* → *I* conversion

Bias currents are shared between ALL the channels

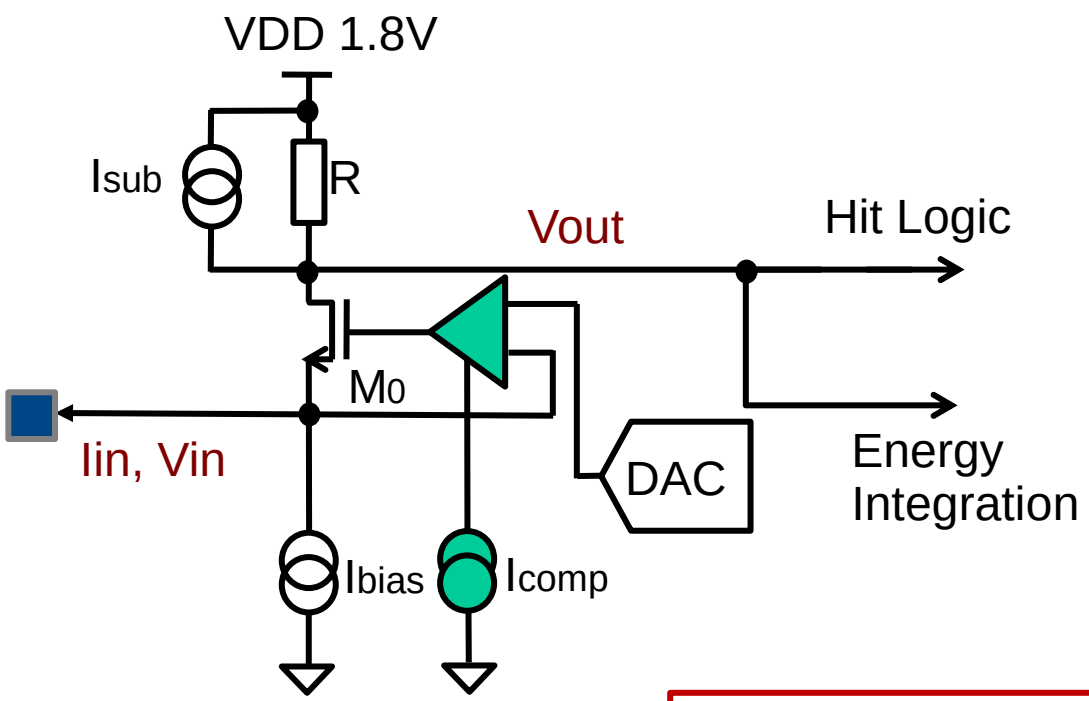
Isub + Ibias ~ 5mA

G = 100 I → U conversion

Input impedance ~ 25- 40Ω

Low pass frequency ~150-200 MHz

Input Stage Design: (2) Regulated Cascode



Active regulation circuit : needs one more current source

→ Icomp > Ibias

→ direct dc setting (span ~1V)

→ lower input impedance

DAC : same as before

Still low power consumption!

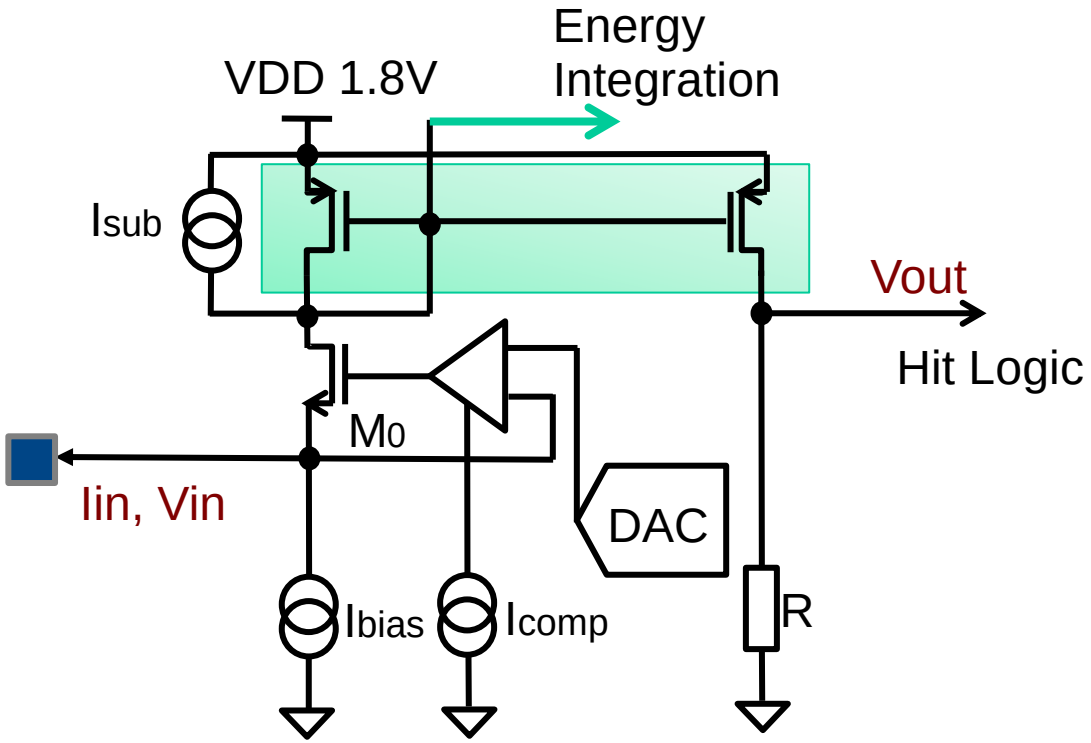
Isub + Ibias + Icomp ~ 7mA

G = 100 I→ U conversion

Input impedance ~ 3Ω

Low pass frequency ~650 MHz

Input Stage Design: (3) Regulated “Mirrored” Cascode



One more “stage”

Current is mirrored (x M)

→ Higher Gain = M x R

→ Larger Dynamic range

→ Direct current injection into the energy integrator

Isub, Ibias, Icomp ~ 7 – 8 mA

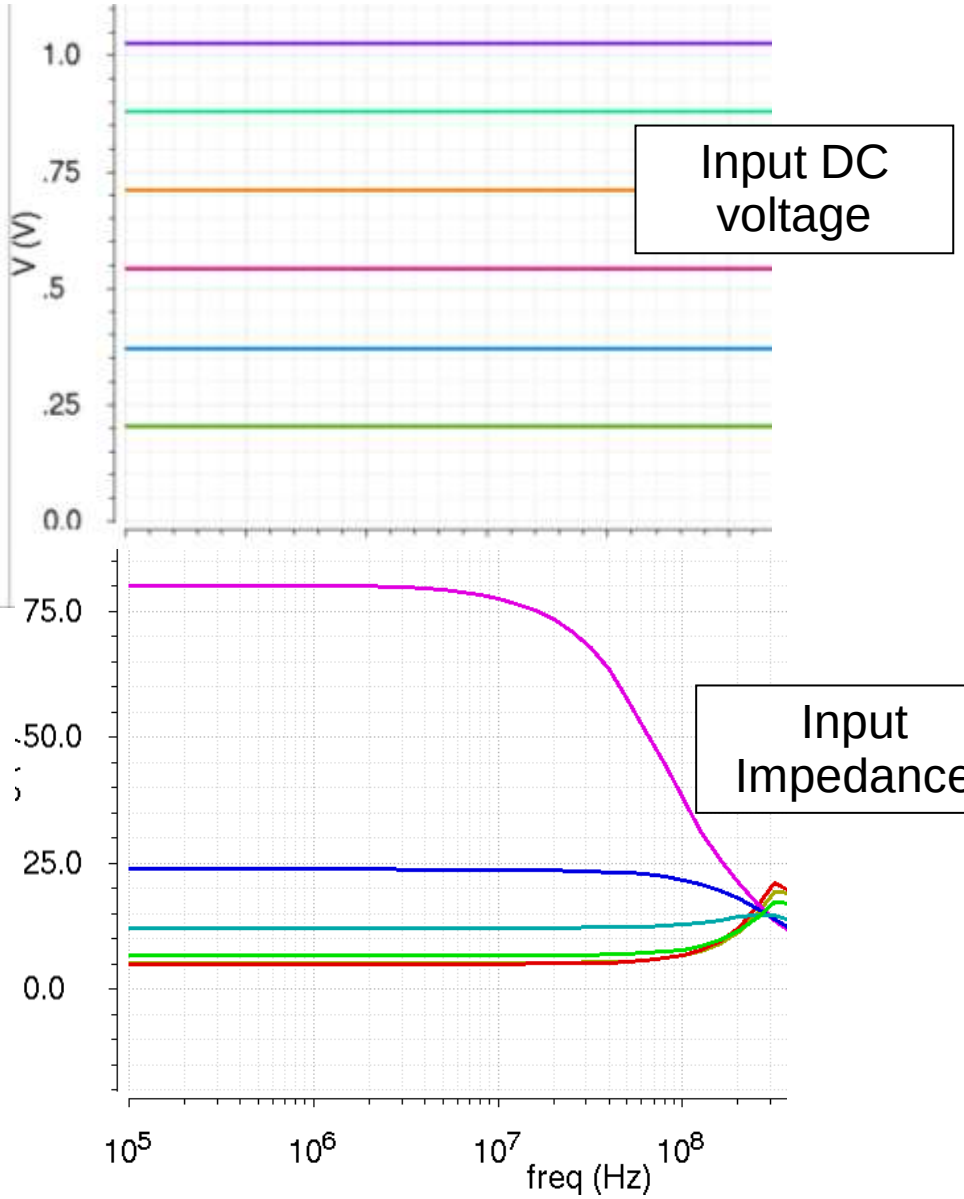
G = M x R

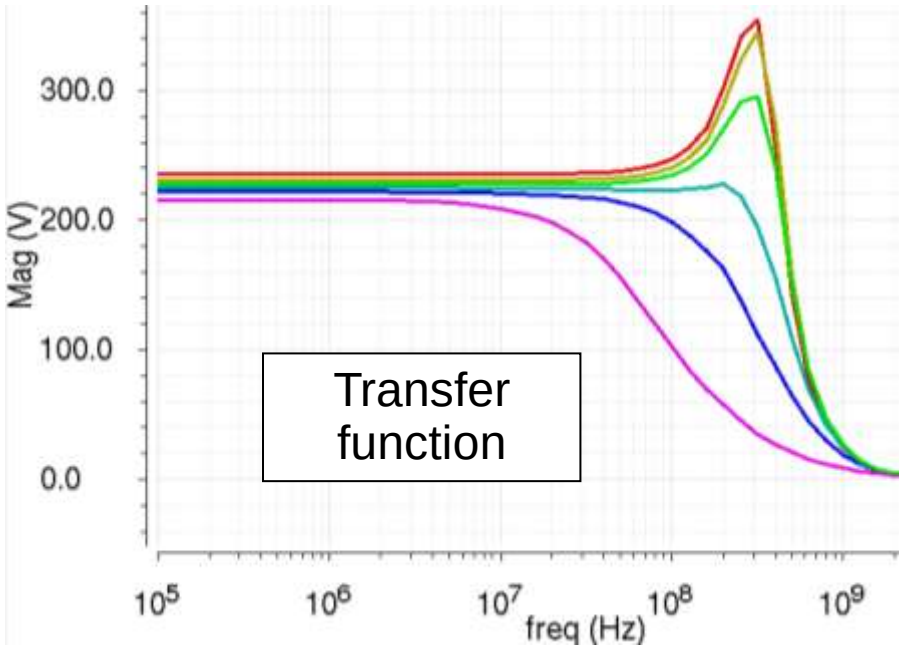
Input impedance ~ 3Ω

Low pass frequency ~650 MHz

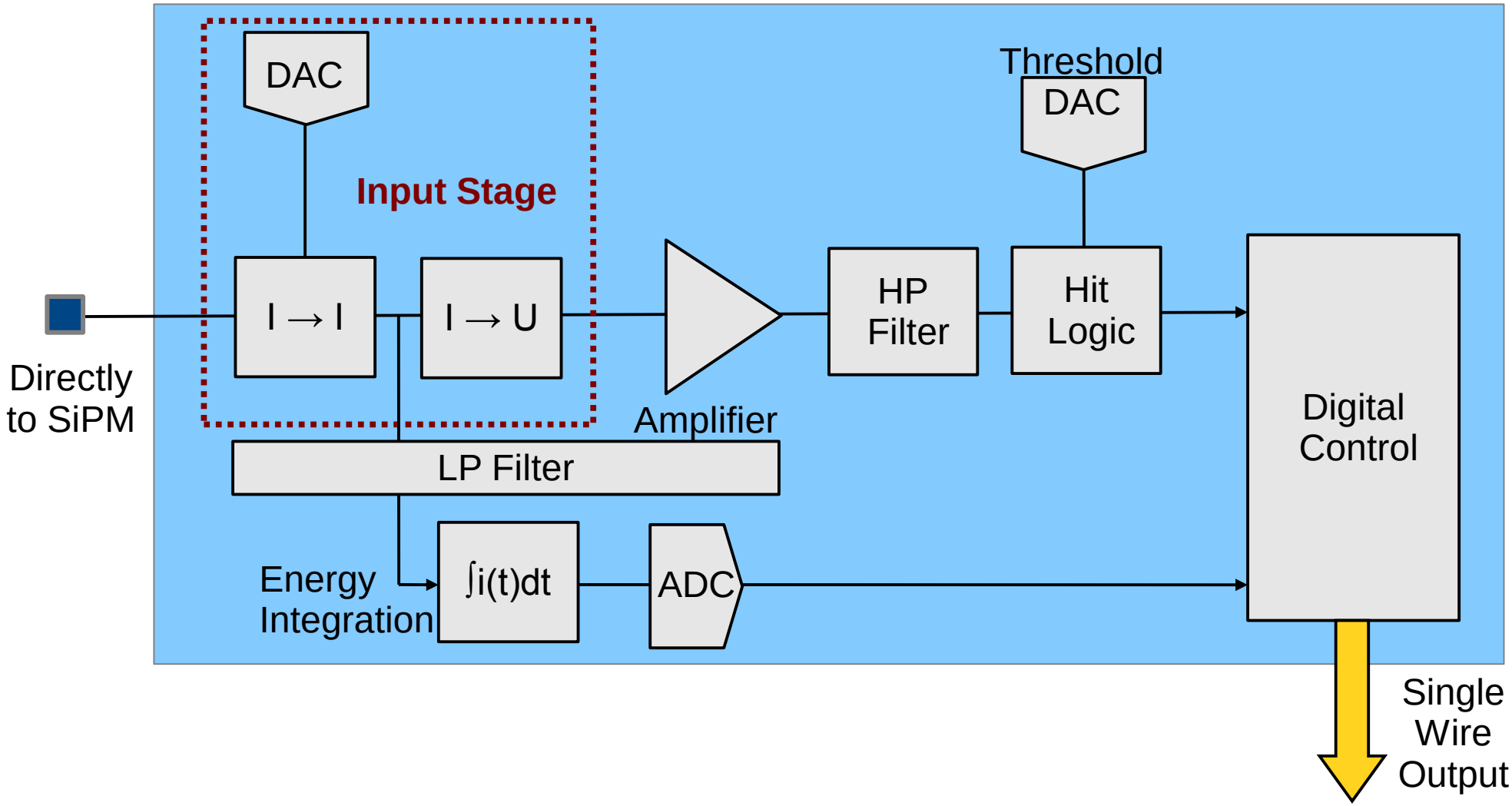
Frontend Design: input DAC effect

Simulation results for different DAC settings:



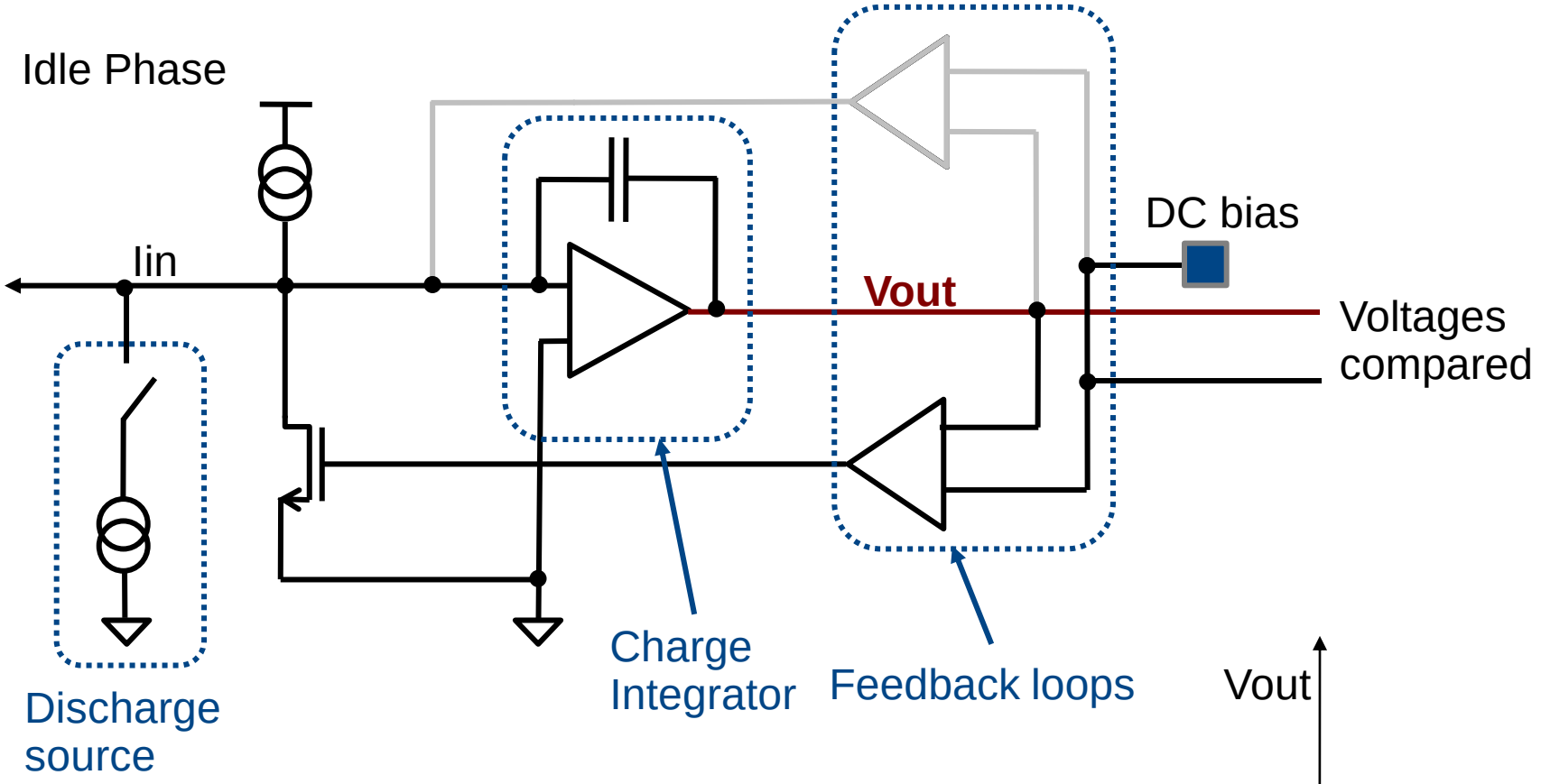


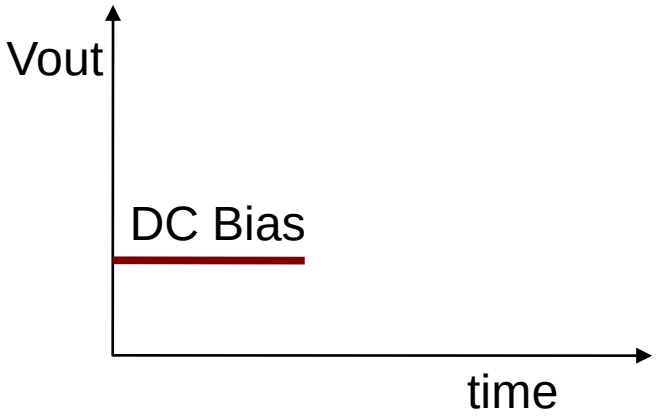
Frontend Design: Channel Architecture



Frontend Design: Energy Integration

The energy integration is performed with a classic charge integrator → the discharge time is a direct measurements of the charge collected



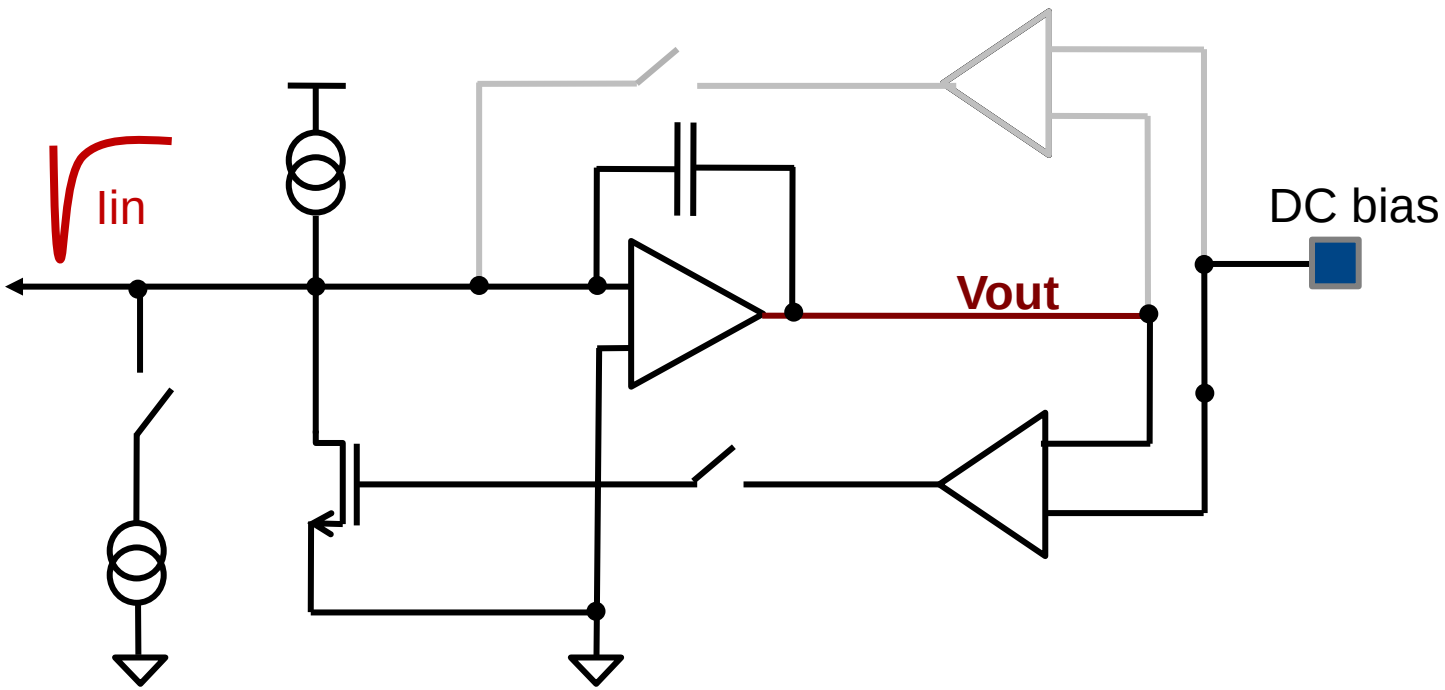


Input current is first integrated

Charge is then measured by constant current discharge.

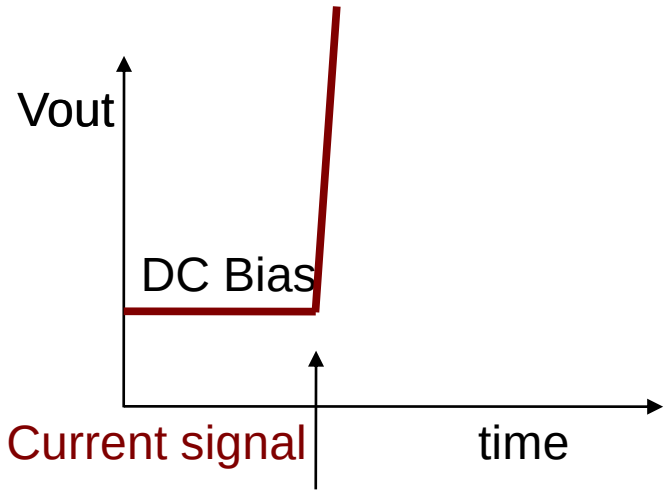
Frontend Design: Energy Integration

Integration Phase



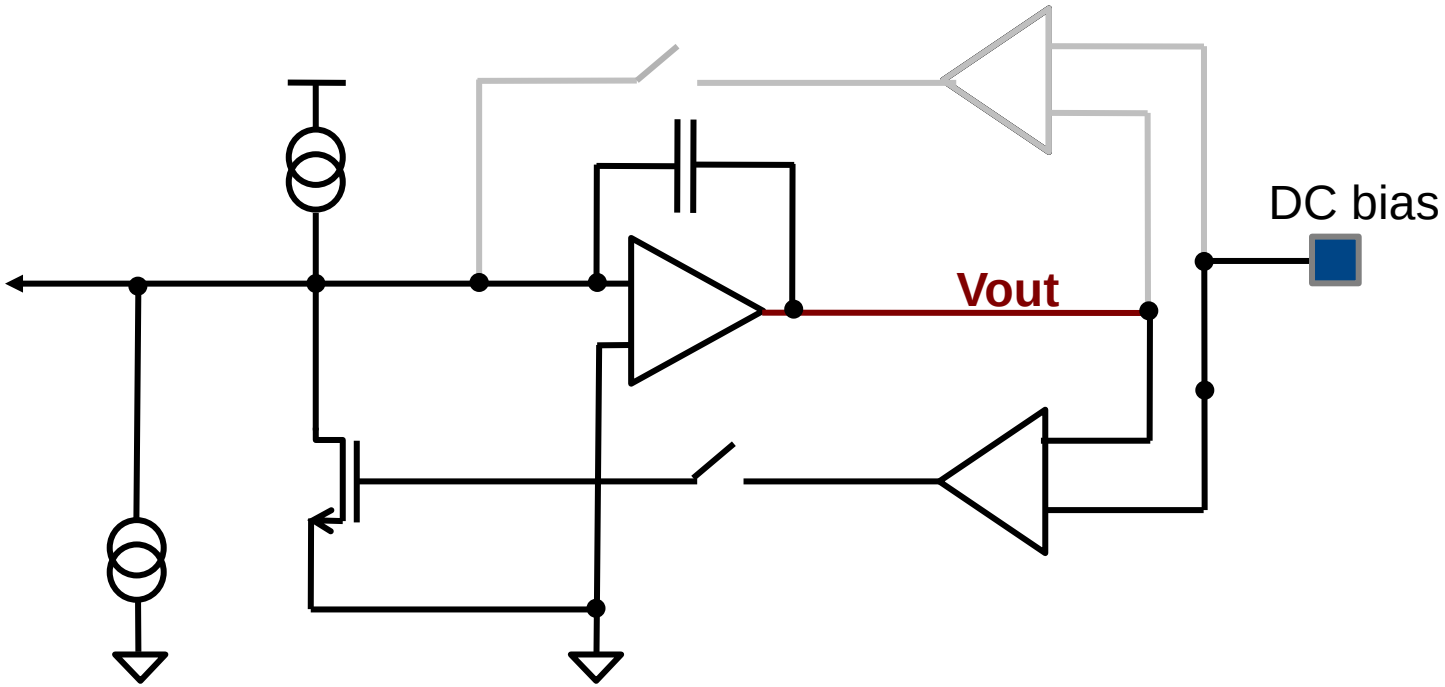
Charge integration starts when a “hit” is detected by the hit logic

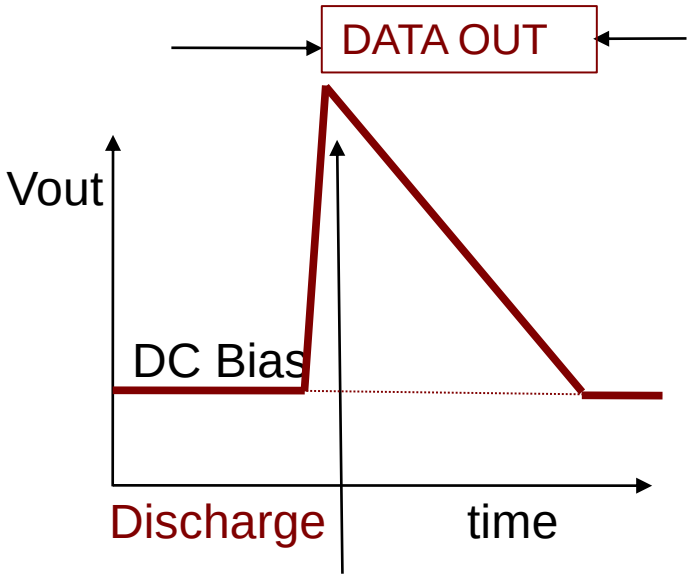
The feedback loops are disabled



Frontend Design: Energy Integration

Discharge Phase

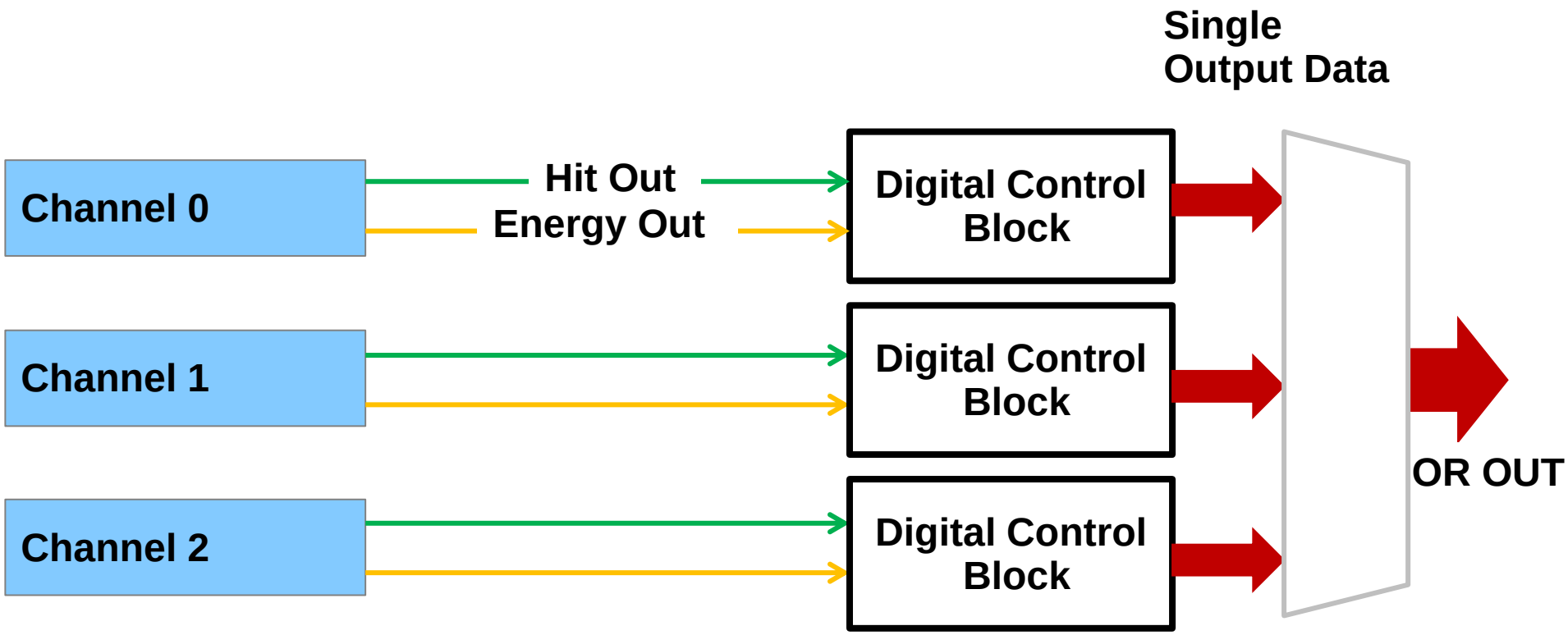




Discharge phase starts after a **programmable delay** → all the charge should be collected on the capacitor

It stops when Vout reaches DC Bias

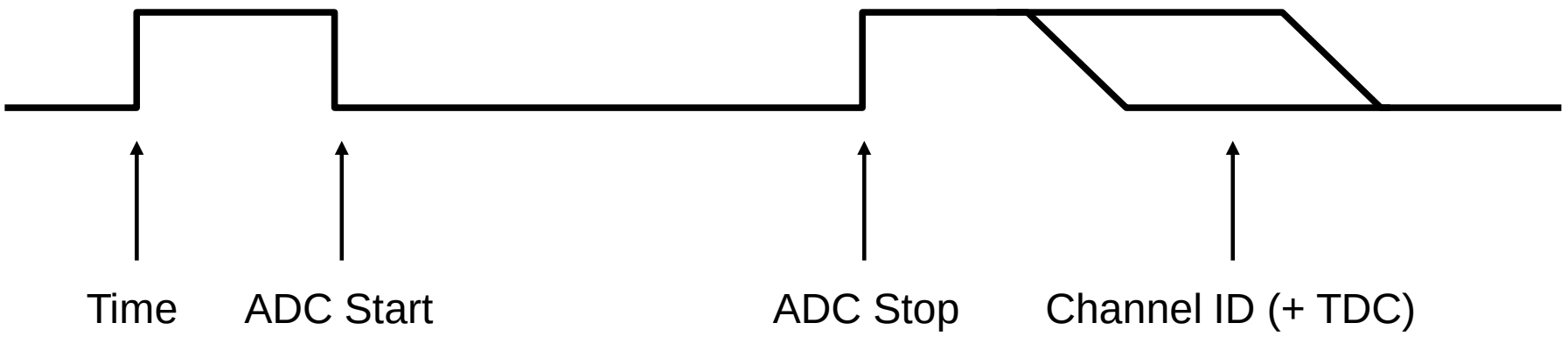
Frontend Design: Single-Wire Output Protocol



The Digital Control Block uses a generated internal clock @ 250 MHz

Time, energy and ID channel information need to be encoded

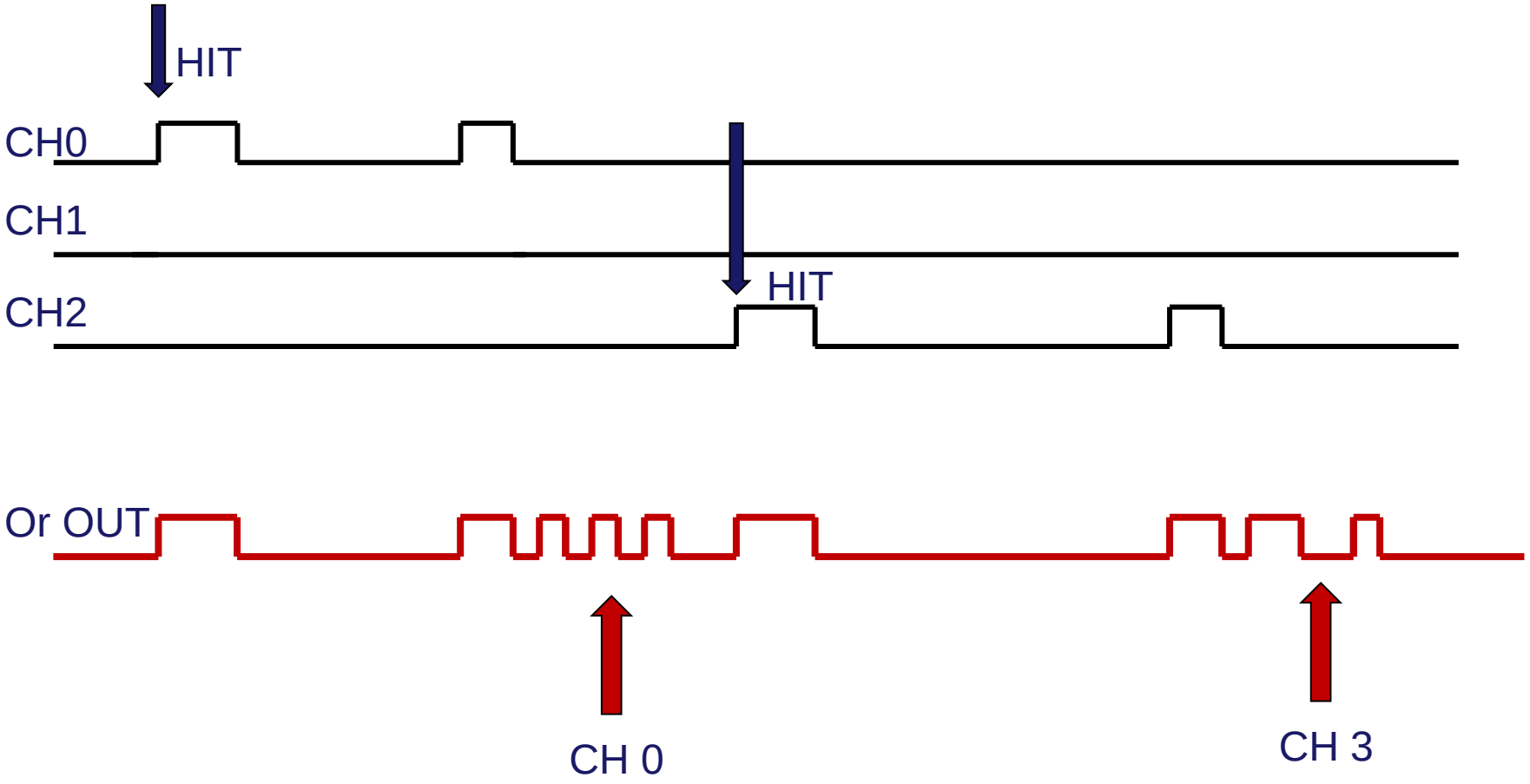
Frontend Design: Single-Wire Output Protocol



- First rising edge: Timing signal
  To be sampled by FPGA with ps-precision.
- Time difference between ADC Start / ADC Stop is the ADC result.
  Approximately proportional to energy.
  To be sampled with ns-precision.
- Channel ID / TDC data

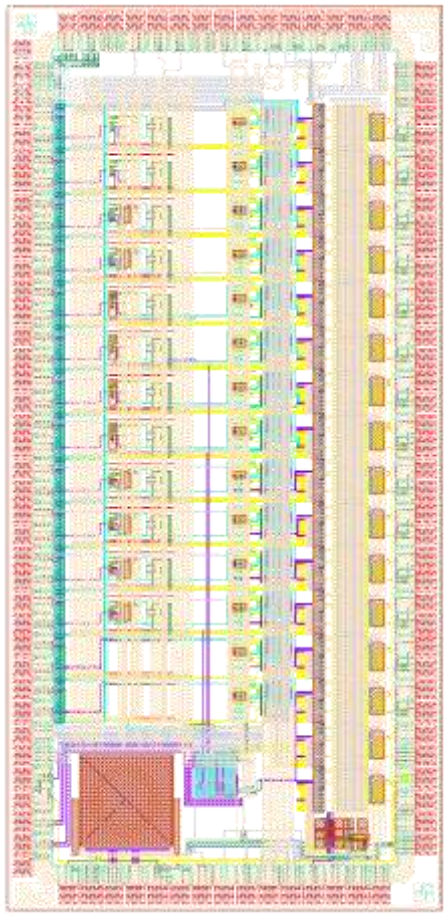
Simulated output:

Frontend Design: Single-Wire Output Protocol



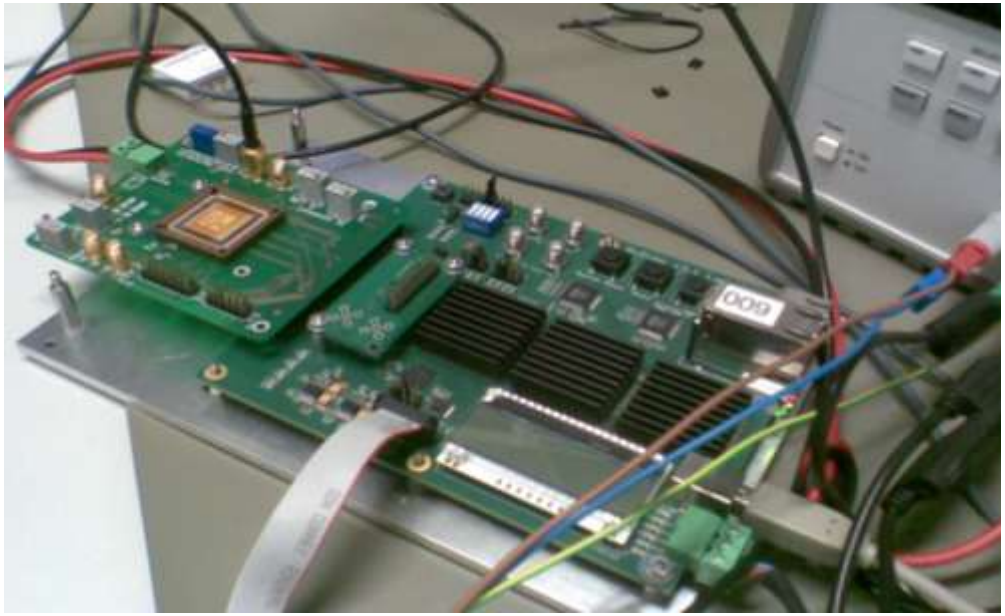
The digital encoded protocol can contain the TDC information as well

Chip Overview



- Six channel designs have been included in the test chip
- Common bias
- A channel pair can be tested per time
- Some channels contain TDC
- LC oscillator generates 250 MHz clock

A TDC on the external FPGA (~50 ps resolution) has been designed for time coincidence measurements

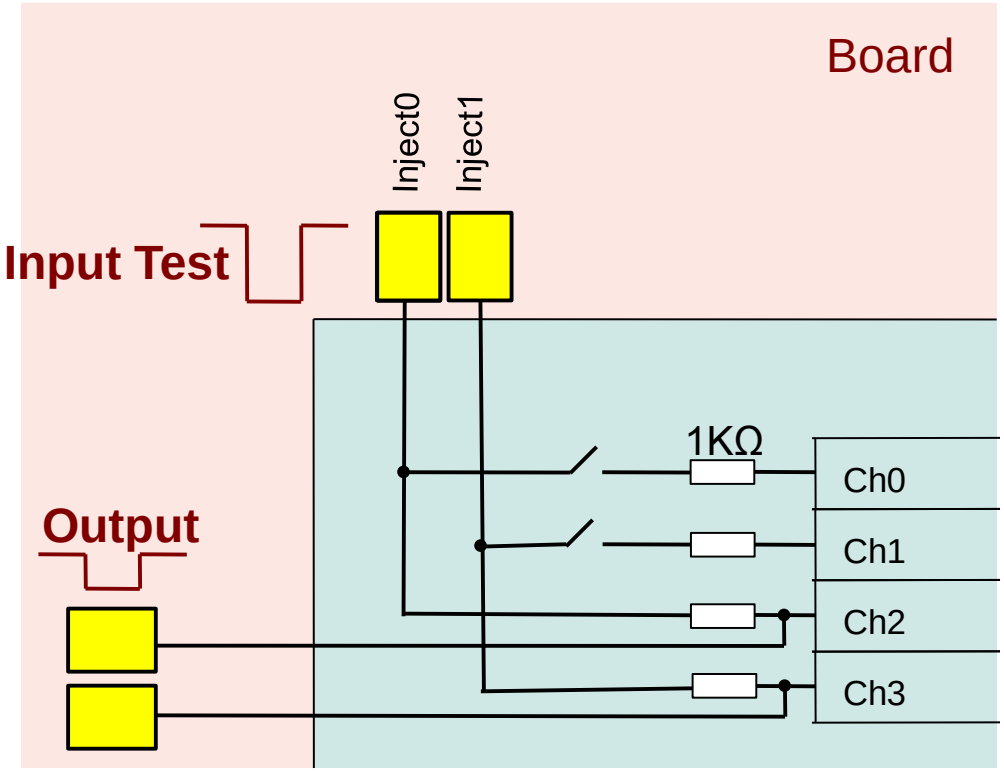


Measurements Results: Input Impedance

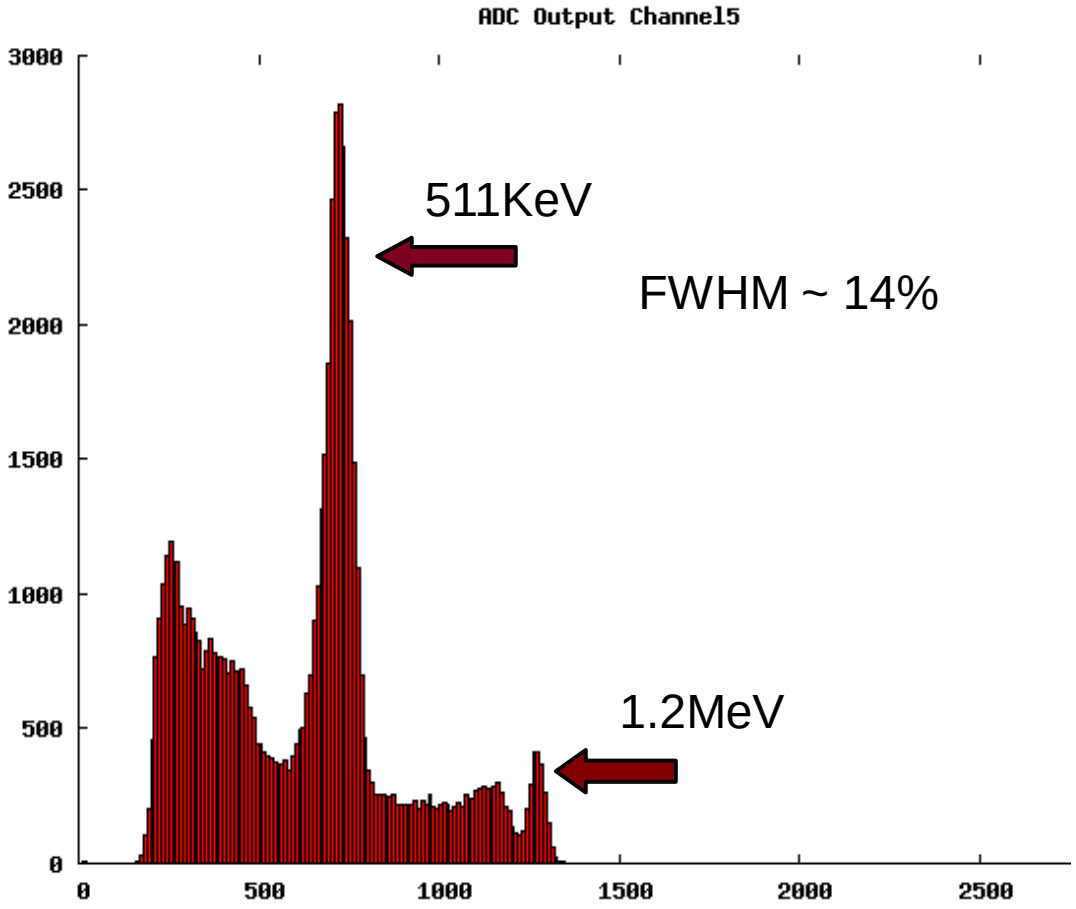
A common injection path through 1KΩ resistor is on-chip for testing purpose

Easy evaluation of the input impedance

- Non compensated channels → ~ 70 Ohms (expected 25-40 Ohms)
- Compensated channels → 7 Ohms (expected 4 Ohms)



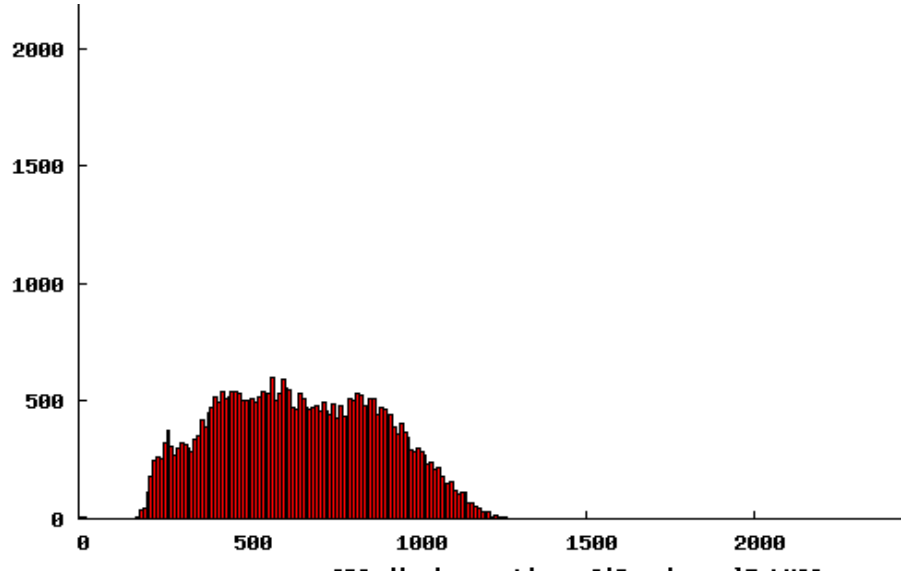
Energy spectrum with LYSO crystal and Na source



FWHM ~ 14%

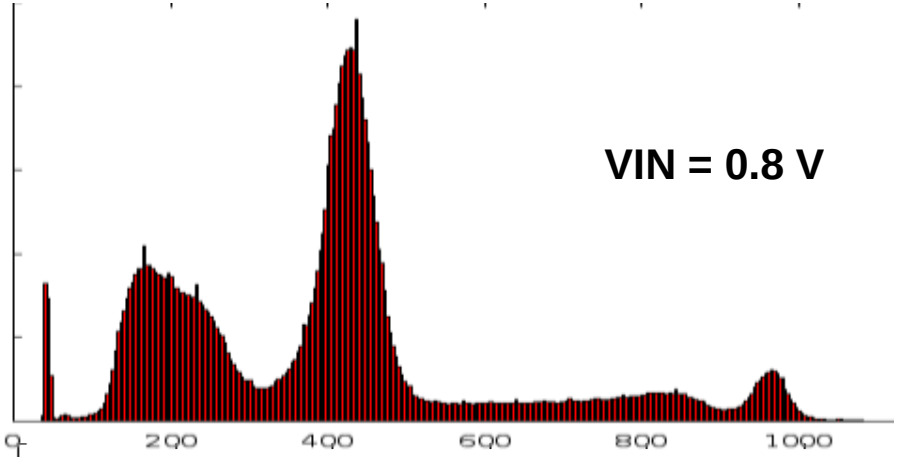
Discharge time (ns)

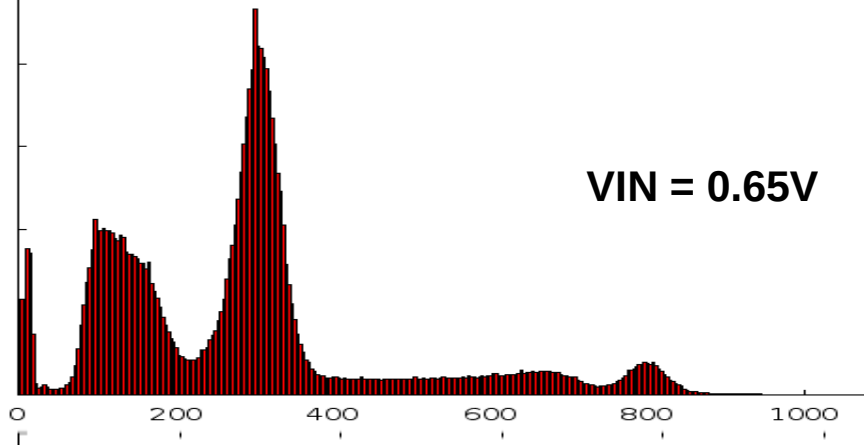
Same setting, only with the LYSO

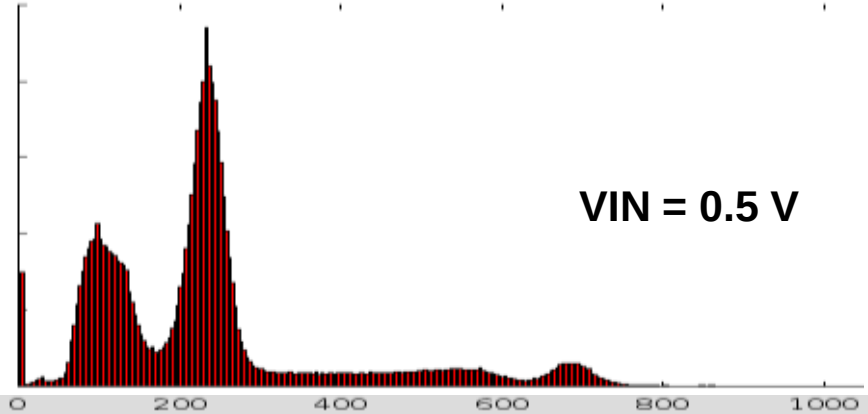


Discharge time (ns)

Measurements Results : effect of input voltage on energy gain





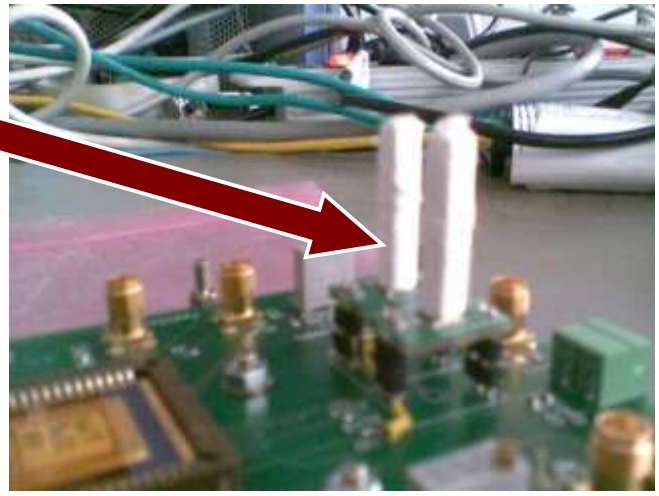


The energy integration gain has an almost **linear dependence** on the DC input voltage

Same channel settings, only the dc input bias changes.
Measurements taken with a non regulated channel

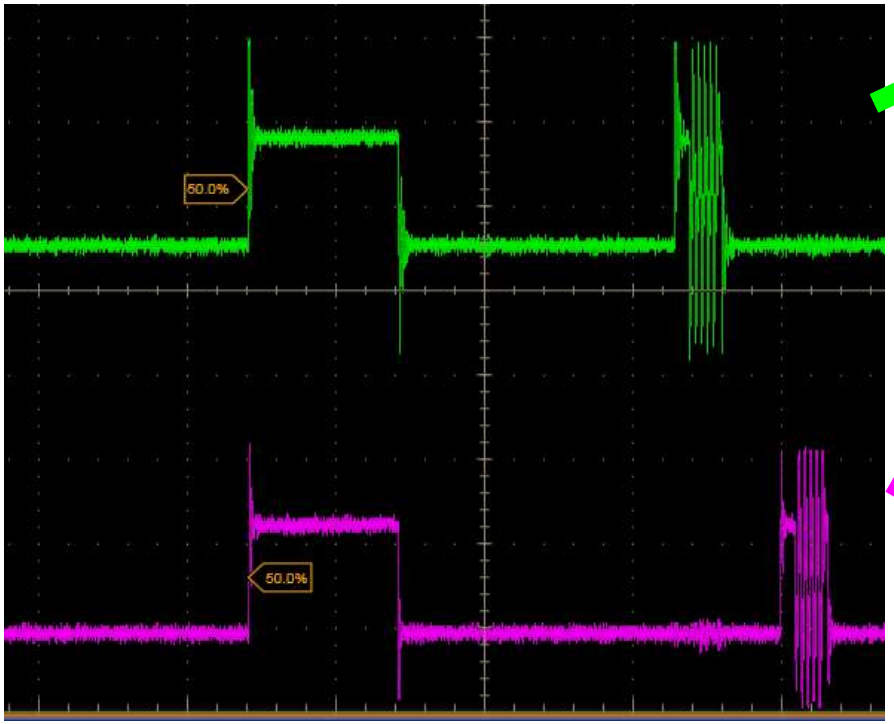
Measurements Results: Time Coincidence

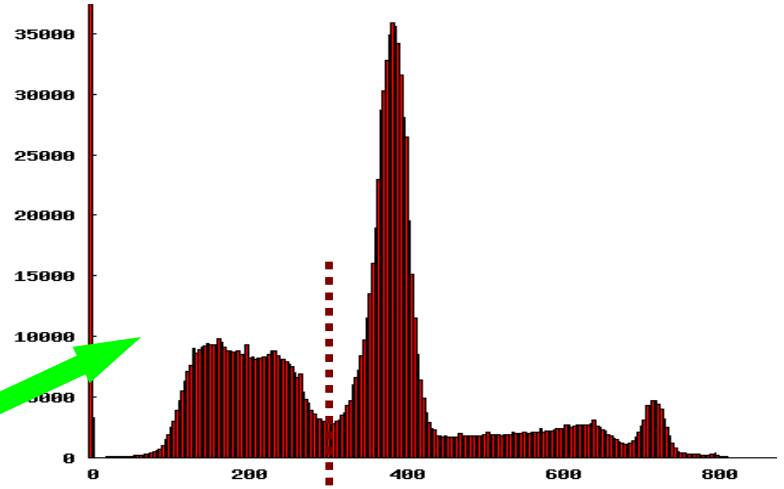
Sodium source
in the middle

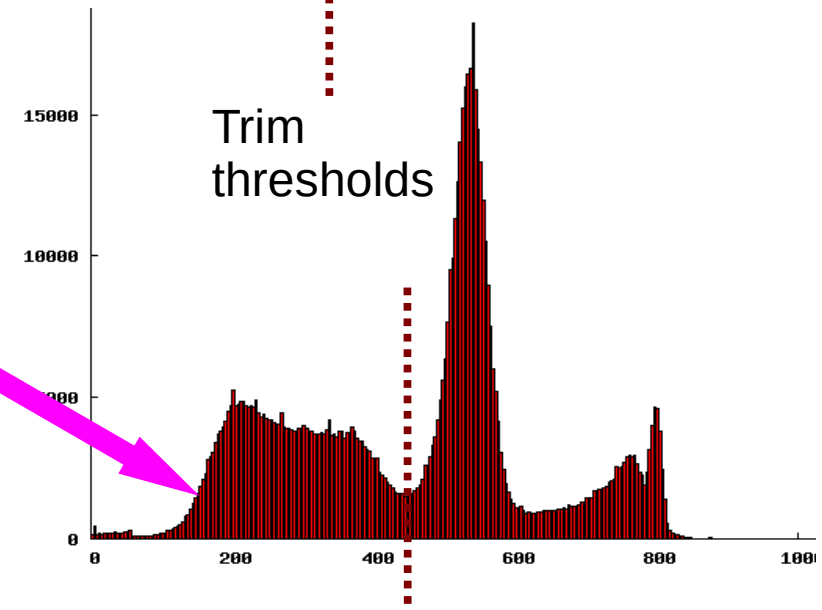


Even

Odd

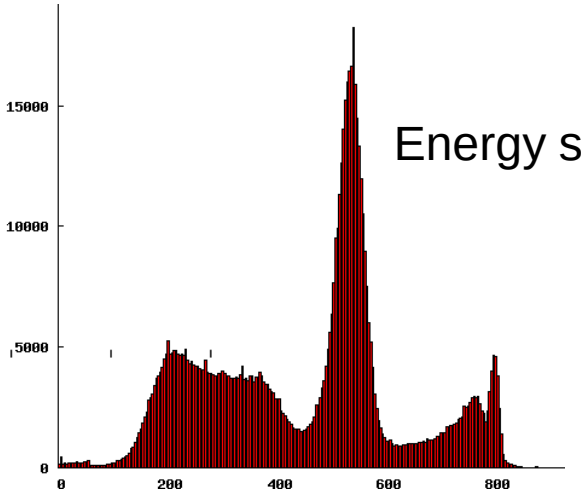




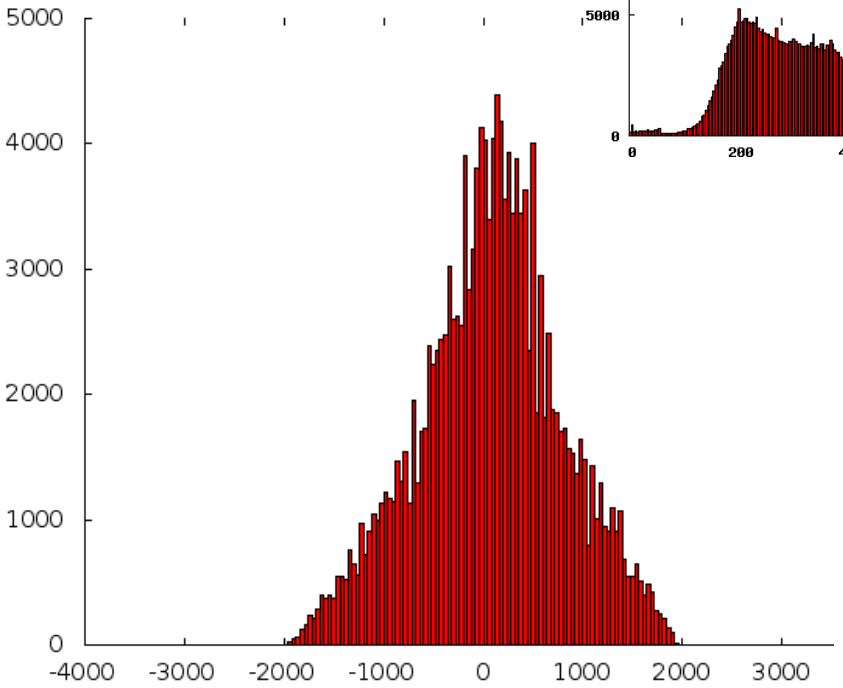


Measurements Results: Time Coincidence

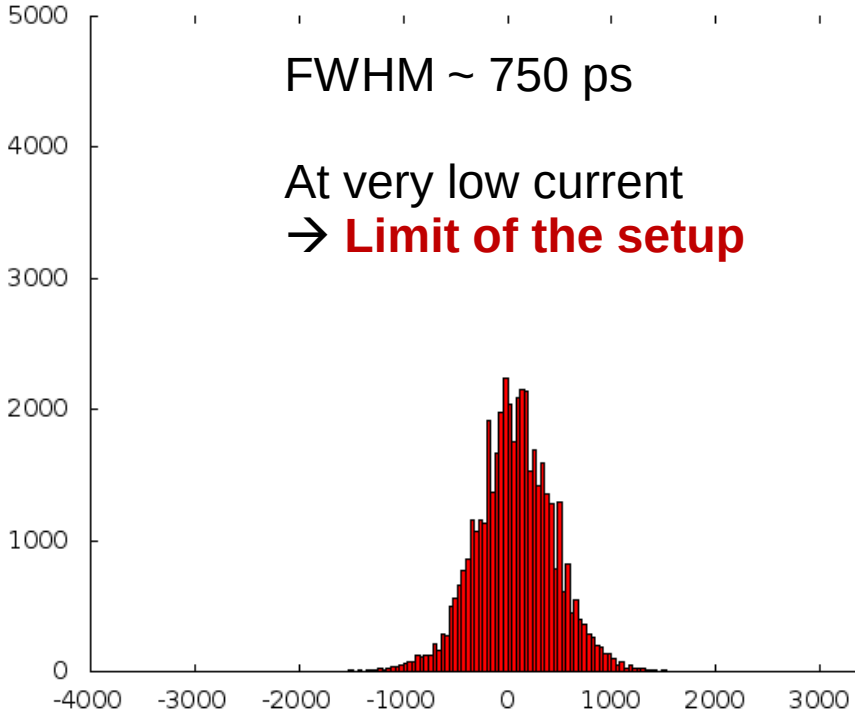
Time coincidence measurement with a low current in the SiPm (about 100 muA in both SiPms)



Energy spectrum



Time coincidence before energy cut



FWHM ~ 750 ps

At very low current
→ **Limit of the setup**

Time coincidence after energy cut

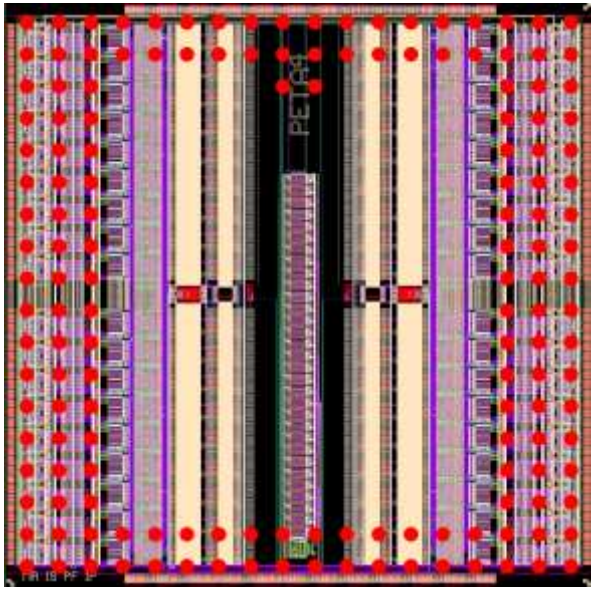
Conclusions

- Starting from HYPERIMAGE module, a new module is under study for better timing resolution, spatial resolution and compactness within SUBLIMA project

HyperImage Module

Next steps:

- PETA4 has been designed and submitted
  - Better timing
  - Higher channel count
  - Bump bonding
- Presented FE for SiPM readout
  - variable DC input
  - low power
  - very low input impedance
  - Simple & low power ADC
  - It works fine and has been integrated in a multi-channels ASIC



Thank you!

Frontend Design: Energy Integrator

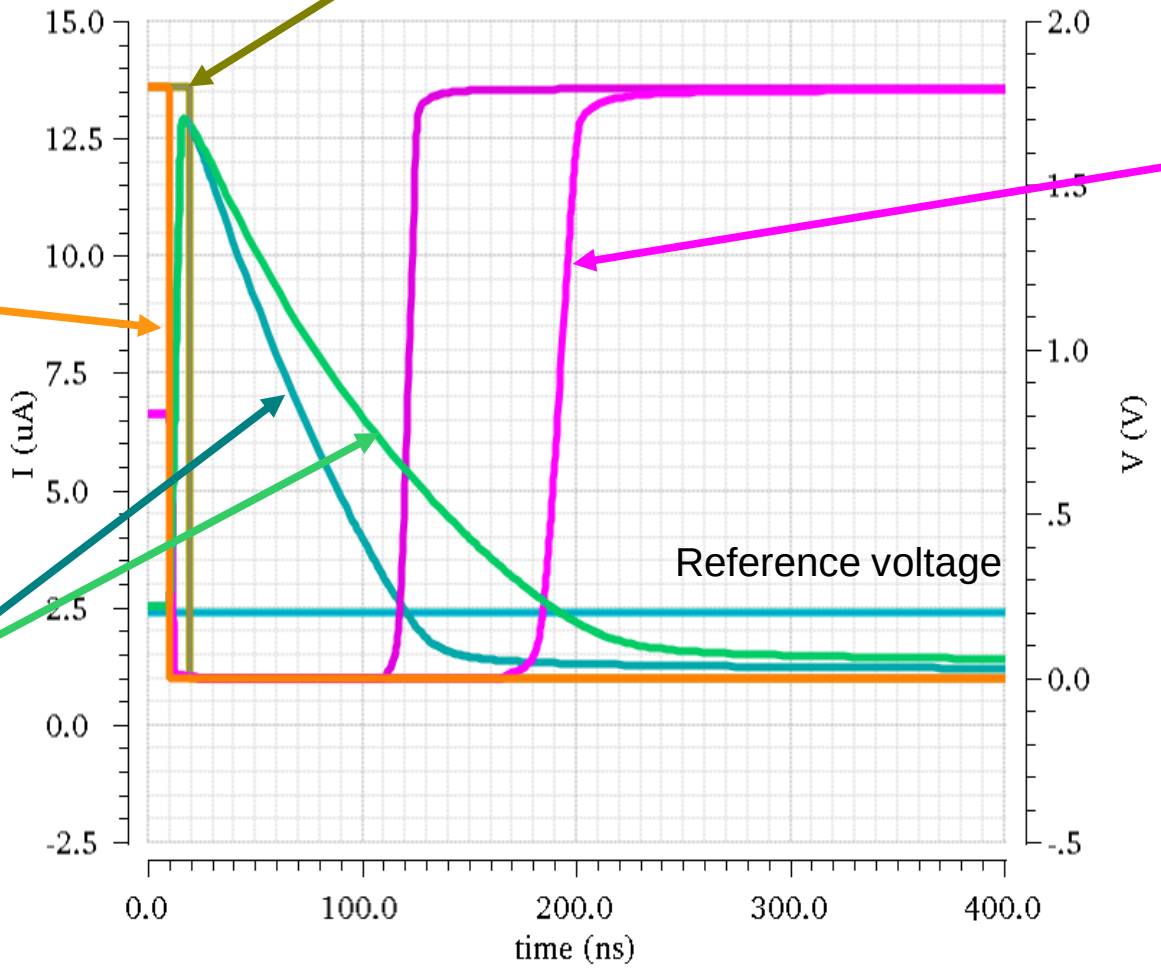
Simulation for two different discharge currents:

After the accumulation of the all charge, the discharge phase starts

When the discharge voltage reaches a reference value, the integration is finished

Signal arrived, the compensation of the integrator is turned off

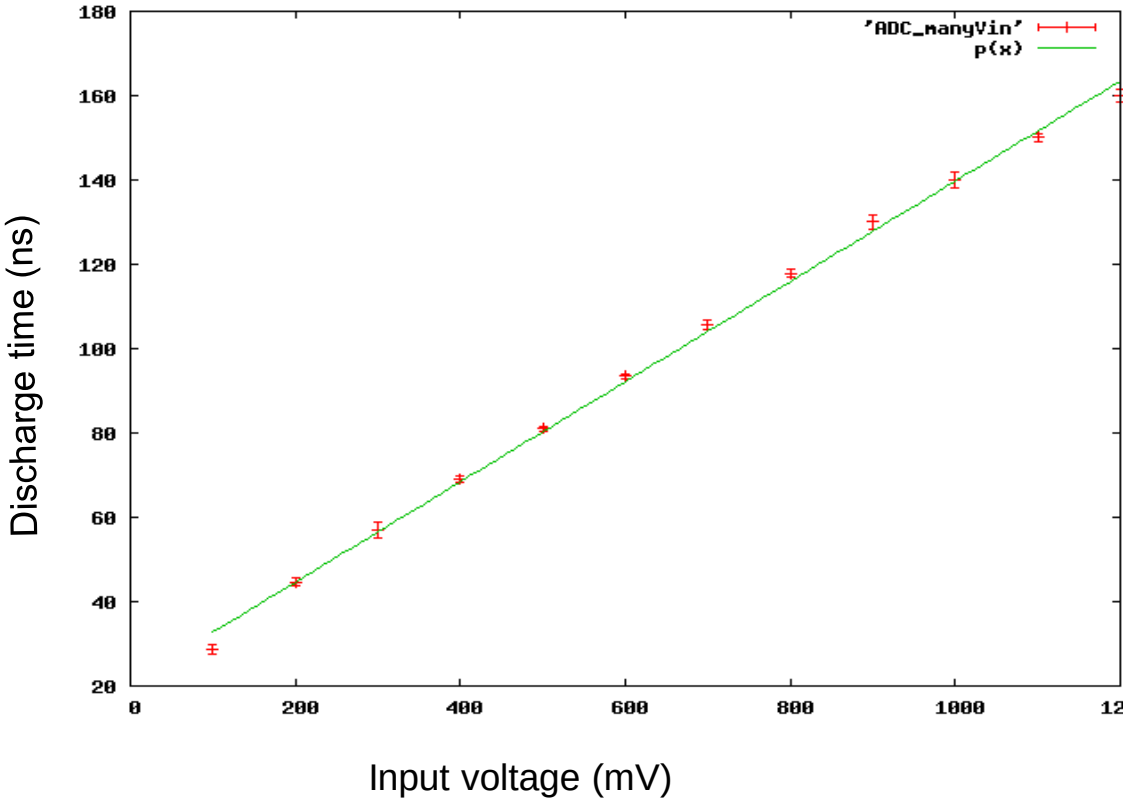
The discharge time is depending on the discharge current



Measurement Results: Energy Integration

Test for ADC linearity

- Voltage pulses at different amplitudes, through the injection path



Readout clock frequency
280 MHz